Hall Ticket Number:

Code No. : 21615

VASAVI COLLEGE OF ENGINEERING *(Autonomous)*, HYDERABAD

M.E. (ECE: CBCS) I-Semester Main Examinations, January-2019

(Embedded Systems & VLSI Design)

Advanced Computer Organization

Time: **3** hours Max. Marks: **60**

*Note: Answer **ALL** questions in **Part-A** and any **FIVE** from **Part-B***

Q.No.	Stem of the question	M	L	CO	PO
	Part-A (10 × 2 = 20 Marks)				
1.	Consider a 4 segment pipeline processor with stage delays 2 ns, 8 ns, 3 ns, 10 ns. Does the pipeline processor belongs to linear or non-linear? Also calculate the time taken to execute 100 tasks in the pipeline processor.	2	2	1	2
2.	Define the terms Instruction Issue Rate(IIR) and Instruction Issue Latency(IIL) w.r.t super scalar processors. Compute the IIR and IIL of a super scalar super pipeline processor of degree (4,3).	2	2	1	2
3.	State the address sequencing capabilities required for the micro programmed control unit.	2	1	2	1
4.	Consider a direct mapped cache of size 32 KB with block size 32 bytes. The CPU generates 32 bit addresses. Find the number of bits needed for cache indexing and the number of tag bits.	2	2	2	2
5.	Increasing the RAM of a computer typically improves performance of the system. Justify the statement.	2	2	3	2
6.	Compute the amount of ROM needed to implement an 8 bit multiplier.	2	2	3	2
7.	How many characters per second can be transmitted over a 4800-baud line in each of the following modes? Assume a character code of eight bits. i) Synchronous serial transmission. ii) Asynchronous serial transmission with one stop bit.	2	2	4	2
8.	An AXI bus has a data width of 64 bits and uses a 200 MHz clock with the bus. Compute the maximum throughput of AXI bus.	2	2	4	2
9.	Draw the instruction format of a vector processor and describe the functionality of each field in the format.	2	2	6	1
10.	On what basis does M.J.Flynn classified the parallel computer systems? Also list them.	2	2	6	1
	Part-B (5 × 8 = 40 Marks)				
11. a)	What are the different types of dependencies possible in a pipelined processor? Describe each type of dependency with an example.	4	2	1	2
b)	Consider a processor having 4 pipeline stages and there are 8 instructions to be executed. Draw the space-time diagrams showing the execution sequence for the following cases (i) Non-overlapped execution and (ii) Overlapped execution. Also compute the number of CPU clock cycles required for each case from the space-time diagrams drawn.	4	3	1	2

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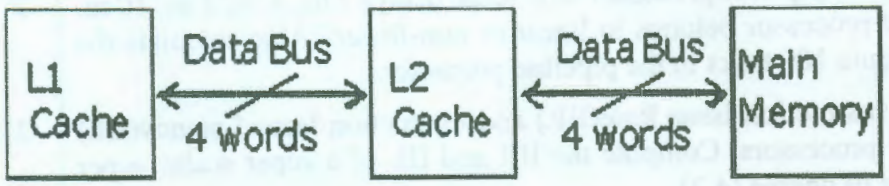
Code No. : 21

12. a)	Based on the type of control word stored in the Control Memory (CM), how do you classify different types of micro-programmed control unit organisations and describe the salient features of each type.	4	3	2	1
b)	A hypothetical processor supports 256 instructions. Each instruction takes 12 cycles to complete the execution. Processor supports horizontal control unit design. It has 24 control signals and 16 flags. Formulate the microinstruction format?	4	4	2	2
13. a)	Describe different application areas of Vector Processors.	4	3	3	3
b)	A computer system has an L1 cache, an L2 cache, and a main memory unit connected as shown below.  The block size in L1 cache is 4 words. The block size in L2 cache is 16 words. The memory access times are 3 nanoseconds, 30 nanoseconds and 300 nanoseconds for L1 cache, L2 cache and main memory unit respectively. When there is a miss in L1 cache and a hit in L2 cache, a block is transferred from L2 cache to L1 cache. Analyse and estimate the time taken for the block transfer from L2 cache to L1 cache?	4	4	3	3
14. a)	Analyze and compare the synchronous and asynchronous serial communication schemes.	4	4	4	3
b)	What is parallel priority interrupt scheme? Design a parallel priority interrupt hardware for a system with four interrupt sources.	4	5	4	2
15. a)	Pipeline and Vector processors require simultaneous access to memory from two or more sources. How do you solve this problem using memory interleaving concept?	4	4	6	3
b)	What is high performance computing? Describe its performance parameters.	4	3	6	2
16. a)	The control memory used in the design of a microprogram control unit has 128 words of 20 bits each. Analyze and compute the following. i) How many bits are there in the control address register? ii) How many bits are there in each of the four inputs that are going into the multiplexers? iii) What are the number of inputs in each multiplexer and how many multiplexers are needed?	4	3	1	2
b)	Analyze and compare the advantages and limitations of hardwired and microprogrammed approaches for designing the control unit of CPU.	4	4	2	3

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Code No. : 21615

17. Answer any ***two*** of the following:				
a) The memory access time is 2 nanosecond for a read operation with a hit in cache, 10 nanoseconds for a read operation with a miss in cache, 3 nanoseconds for a write operation with a hit in cache and 15 nanoseconds for a write operation with a miss in cache. Execution of a sequence of instructions involves 200 instruction fetch operations, 120 memory operand read operations and 80 memory operand write operations. The cache hit-ratio is 0.95. Analyse and compute the average memory access time (in nanoseconds) in executing the sequence of instructions.	4	4	3	3
b) Consider the following description of a protocol of input device communication. i) Each device has a distinct address ii) The bus controller scans each device in sequence of increasing address value to determine if the entity wishes to communicate. iii) The device ready to communicate leaves it data in IO register. iv) The data is picked up and the controller moves to step-a above. Analyze and identify the form of communication that best describes the IO mode.	4	5	4	3
c) Explain the following shared memory multiprocessors organization with neat sketch. i) Uniform Memory Access(UMA) ii) Non- Uniform Memory Access iii) Cache Only Memory Access(COMA)	4	3	6	2

M: Marks; L: Bloom's Taxonomy Level; CO: Course Outcome; PO: Programme Outcome

S. No.	Criteria for questions	Percentage
1	Fundamental knowledge (Level-1 & 2)	40%
2	Knowledge on application and analysis (Level-3 & 4)	50%
3	*Critical thinking and ability to design (Level-5 & 6) (*wherever applicable)	10%

Hall Ticket Number:

Code No.: 21514

VASAVI COLLEGE OF ENGINEERING *(Autonomous)*, HYDERABAD

M.E. (ECE: CBCS) I-Semester Main Examinations, January-2019

(Communication Engineering & Signal Processing)

Image and Video Processing

Time: 3 hours Max. Marks: 60

Note: Answer ALL questions in Part-A and any FIVE from Part-B

Q. No	Stem of the Question	M	L	CO	PO
	Part-A (10 × 2 = 20 Marks)				
1.	What is neighbourhood criterion of an image?	2	1	1	1
2.	List the required conditions for a function to be act as wavelet.	2	5	1	2
3.	Why segmentation is needed in an image processing?	2	4	2	2
4.	Write a mask for mean filter and what is effect of it on an image?	2	4	2	2
5.	Draw the general model for image compression.	2	3	3	2
6.	Define the terms coding and spatial redundancy.	2	3	3	2
7.	How do you sample the given video?	2	2	4	2
8.	Name different video standards.	2	1	4	2
9.	How motion vector is used in video processing?	2	3	5	2
10.	Compare mesh based and block based motion estimation methods.	2	2	5	2
	Part-B (5 × 8 = 40 Marks)				
11. a)	Explain the basic steps in image processing with neat block diagram and examples.	6	2	1	1,2
b)	Derive the relation between DCT and DFT.	2	5	1	2
12. a)	Explain any four point processing techniques for image enhancement.	4	2	2	2
b)	Describe the split and merge method to segment the given image.	4	2	2	2
13. a)	Encode the 4-bit image $f(m,n)=\begin{bmatrix}8 & 8 & 7 & 6\\ 8 & 8 & 6 & 7\\ 5 & 5 & 5 & 5\\ 5 & 8 & 8 & 8\end{bmatrix}$ using Huffman coding and compute its compression ratio.	4	4	3	2
b)	Analyse and compare the performance of Run-length coding and Lossless predictive coding.	4	4	3	2
14. a)	Draw the block diagram of time-varying image formation model and explain in detail.	4	2	4	3
b)	List the different three dimensional models used in video processing and explain.	4	2	4	3

Contd... 2

15. a)	Explain pixel based method to estimate motion vector in video processing and compare it with global motion method.	4	2	5	3
b)	Derive the optical flow equation.	4	2	5	3
16. a)	Define Discrete Wavelet Transform and determine the forward Haar transform of image $f(m,n)=\begin{bmatrix}4 & 6\\ 8 & 8\end{bmatrix}$.	4	4	1	2
b)	How an edge in an image is detected and explain any one of such method?	4	4	1	2
17.	Answer any ***two*** of the following:				
a)	Explain the transform coding for image compression with neat block diagram.	4	2	3	2
b)	Illustrate the photometric image formation method with suitable equations.	4	2	4	2
c)	Describe the region based motion estimation method in video processing.	4	2	5	2

M: Marks; L: Bloom's Taxonomy Level; CO: Course Outcome; PO: Programme Outcome

S. No.	Criteria for questions	Percentage
1	Fundamental knowledge (Level-1 & 2)	65%
2	Knowledge on application and analysis (Level-3 & 4)	30%
3	*Critical thinking and ability to design (Level-5 & 6) (*wherever applicable)	5%

Hall Ticket Number:

Code No. : 21914

VASAVI COLLEGE OF ENGINEERING *(Autonomous)*, HYDERABAD

M.Tech. (CSE: CBCS) I-Semester Main Examinations, January-2019

Advanced Operating Systems

Time: **3** hours Max. Marks: **60**

*Note: Answer **ALL** questions in **Part-A** and any **FIVE** from **Part-B***

Q. No	Stem of the Question	M	L	CO	PO
	Part-A (10 × 2 = 20 Marks)				
1.	List the limitations of distributed systems.	2	2	1	1
2.	How can you justify whether two events a & b are causally related?	2	3	1	1,2
3.	Differentiate between centralized Deadlock detection and distributed dead lock detection.	2	2	2	1
4.	Find the system throughput for mutual exclusion algorithm if the parameters of synchronization delay=6ms and average critical section execution time=5ms.	2	3	2	1,2
5.	What are the design issues of Distributed File System?	2	2	3	1
6.	List the Coherence protocols.	2	2	3	1
7.	What is Backward error recovery in concurrent systems?	2	2	4	1
8.	How Access Matrix prevents unauthorized access of resources?	2	3	4	1,2
9.	Compute the average turnaround time for the following processes having burst times are P1=21, P2=3, P3=6 using First come first serve scheduling algorithm.	2	3	5	1,2
10.	What way Multiprocessor Operating Systems are different from single Processor Operating System?	2	2	5	1
	Part-B (5 × 8 = 40 Marks)				
11. a)	Draw the architecture of Distributed systems and explain.	4	2	1	1,2
b)	Explain the design issues in distributed operating system.	4	2	1	1,2
12. a)	Explain the Ricart-Agrawala algorithm.	4	2	2	1,2
b)	Show the possibility of Deadlock using graph model.	4	3	2	1,2
13. a)	Explain Load Distributing algorithms in distributed scheduling.	4	2	3	1,2
b)	Draw the architecture of Sun Network file system and explain.	4	3	3	1,2
14. a)	Explain the mutual authentication using Kerberos with neat diagram.	4	2	4	1,2
b)	Consider the following page reference string 1,2,3,4,2,1,5,6,2,1,2,3,76,3,2,14,1 how many page faults would occur for the following replacement algorithms assuming 3 frames i) LRU page replacement ii) Optimal page replacement.	4	3	4	1,2

Contd...2

Code No. : 21914

15. a)	Explain the Inter connection networks for Multiprocessor Systems.	3	2	5	1,2
b)	Assume you have the following jobs to execute with one processor, with the jobs arriving in the order listed here	5	3	5	1,2

Jobs	Arrival time	Burst time
J1	1	6
J2	0	3
J3	2	4
J4	3	2

Calculate average waiting time of jobs by using Shortest job First –Preemptive scheduling algorithm.

16. a)	Explain Logical clocks and Vector clock with examples.	4	2	1	1,2
b)	Justify your answer "Deadlock detection and handling is better than Deadlock prevention".	4	3	2	1,2
17.	Answer any ***two*** of the following:				
a)	Explain about Memory coherence in Distributed shared memory.	4	2	3	1
b)	Illustrate the requirements of Public Key Cryptography?	4	3	4	1,2
c)	Discuss about the motivation behind multiprocessor System.	4	2	5	1

M: Marks; L: Bloom's Taxonomy Level; CO: Course Outcome; PO: Programme Outcome

S. No.	Criteria for questions	Percentage
1	Fundamental knowledge (Level-1 & 2)	60%
2	Knowledge on application and analysis (Level-3 & 4)	40%
3	*Critical thinking and ability to design (Level-5 & 6) (*wherever applicable)	---

Hall Ticket Number:

Code No. : 21614

VASAVI COLLEGE OF ENGINEERING *(Autonomous)*, HYDERABAD

M.E. (ECE: CBCS) I-Semester Main Examinations, January-2019

(Embedded Systems & VLSI Design)

Analog IC Design

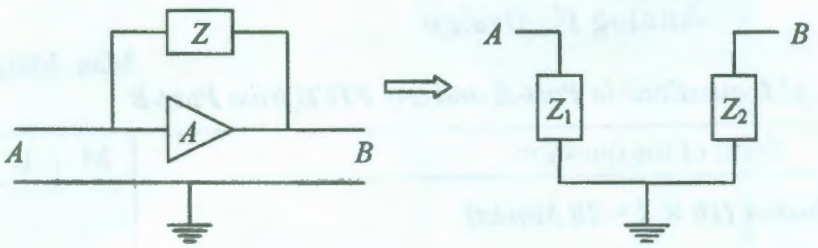
Time: 3 hours Max. Marks: 60

*Note: Answer **ALL** questions in **Part-A** and any **FIVE** from **Part-B***

Q.No.	Stem of the question	M	L	CO	PO
	Part-A (10 × 2 = 20 Marks)				
1.	Mention any two analog functions and explain them briefly.	2	2	2	1
2.	Sketch the structure of a diffused resistor in BJT Technology.	2	2	4	1
3.	Starting from I_d-V_d relation of the nMOSFET in saturation region derive the value of dynamic resistance.	2	3	3	2
4.	Mention any two applications of current mirrors in realizing IC amplifiers.	2	2	4	2
5.	How do you realize a voltage proportional to absolute temperature (PTAT)?	2	5	4	3
6.	Draw the circuit diagram of a single stage C.S. amplifier with current source load and explain briefly.	2	2	3	2
7.	Explain the term "CMRR" in connection with differential amplifier.	2	2	2	1
8.	Describe any two methods of increasing the "Phase margin" of an amplifier.	2	2	4	2
9.	Give the significance of "Crossover frequency" connected with noise in MOSFETs.	2	2	2	1
10.	How do you obtain frequency conversion using a BJT or FET?	2	2	4	2
	Part-B (5 × 8 = 40 Marks)				
11. a)	Differentiate between the sources responsible for "depletion capacitance" and diffusion capacitance in junction diode.	4	4	4	2
b)	Show that the diffusion capacitance varies as the forward current of the diode.	4	4	1	2
12. a)	Describe any three short channel effects in MOSFETs.	2	3	4	1
b)	What are the various types of applications that the current mirrors can be used?	3	4	4	2
c)	Write the specifications of current mirrors and explain their significance.	3	3	4	3
13.	Draw a typical circuit diagram of a "band gap reference" and explain with the help of a derivation.	8	3	3,4	2,3
14. a)	Discuss the role of C.G. amplifier stage in a cascode amplifier?	2	2	4	2
b)	Draw the circuit diagram of cascode amplifier and explain.	3	4	2	1
c)	The gm of the transistors is 2000μ A/V and the load resistance is 50,000Ω. Calculate the voltage gain. What is the approximate output impedance if rds=1.0μΩ.	3	2	1	2

Contd... 2

Code No. : 21614

15. a) Describe a circuit which generates an output current proportional to difference in two input currents, using current mirrors.	4	5	4	3
b) In the following calculate Z_1 and Z_2 in terms of A and Z ($A = \frac{V_B}{V_A}$). 	3	4	1	1
c) Show that $Z_2 \simeq Z$ if A is large.	1	3	2	2
16. a) What is the source for flicker noise in electron devices? Specifically what are the sources of flicker noise in MOSFETs?	4	2	4	1
b) Describe the features of flicker noise.	2	4	4	2
c) Define what is "Crossover Frequency" in MOSFETs and estimate it in terms of relevant FET parameters.	2	3	1	2
17. Answer any ***two*** of the following:				
a) In a three stage phase shift oscillator (in a ring form) $\omega_p = 2\Pi \times 10^4$ rad/sec. calculate the oscillator frequency (W_{sc}) and the voltage gain of each stage.	4	2	1	2
b) Mention the specifications of a frequency convertor and explain their significance.	4	4	3	2
c) Compare CS, CG and CD amplifiers.	4	3	3	2

M: Marks; L: Bloom's Taxonomy Level; CO: Course Outcome; PO: Programme Outcome

S. No.	Criteria for questions	Percentage
1	Fundamental knowledge (Level-1 & 2)	40%
2	Knowledge on application and analysis (Level-3 & 4)	50%
3	*Critical thinking and ability to design (Level-5 & 6) (*wherever applicable)	10%

Hall Ticket Number:

Code No. : 21712

VASAVI COLLEGE OF ENGINEERING *(Autonomous)*, HYDERABAD

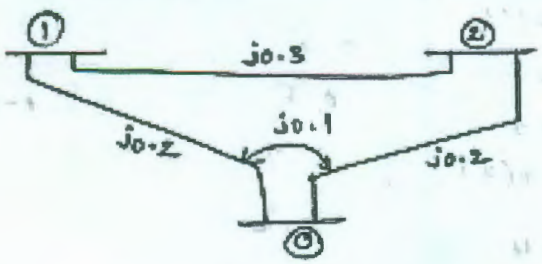
M.E. (EEE: CBCS) I-Semester Main Examinations, January-2018

(Power Systems & Power Electronics)

Advanced Computer Methods in Power Systems

Time: **3** hours Max. Marks: **60**

*Note: Answer **ALL** questions in **Part-A** and any **FIVE** from **Part-B***

Q. No	Stem of the Question	M	L	CO	PO
	Part-A (10 × 2 = 20 Marks)				
1.	Define the following terms i) Link ii) Basic loop	2	1	1,2	1
2.	Show that $A_b K^t = U$	2	2	1,2	1,2
3.	What do you mean by triangularization?	2	1	1,2	1,2
4.	Write expressions for Z_{qi} and Z_{qq} when added element is a branch. Assume P is reference node?	2	2	1,2	1,2
5.	What is the importance of load flow studies in power systems?	2	2	3	1,3
6.	What is acceleration factor? In which method of load flow this factor is recommended?	2	2	3	1,3
7.	Write the importance of Clark's transformation matrix?	2	2	1,2	1,2
8.	Write the equations for Z_{ll}^{abc} and Z_{ll}^{abc}	2	3	1,2	1,2
9.	What are the different types of faults and write the effect of each fault on the power system?	2	2	2	1,2
10.	Estimate the fault level when a fault takes place in power system?	2	3	1,2	1,2
	Part-B (5 × 8 = 40 Marks)				
11. a)	The transpose of the matrix A is given by $A^t = \begin{bmatrix} -1 & 1 & 0 & 1 & 0 & 0 \\ 0 & -1 & 1 & 0 & 0 & 0 \\ 0 & 0 & -1 & -1 & 1 & 0 \\ 0 & 0 & 0 & -1 & 1 & 1 \end{bmatrix}$ Draw its oriented graph and obtain B, $\bar{B}$, C, $\bar{C}$ and K matrices of the network?	6	4	1,2	1,2
b)	Write the equation for Zloop by singular transformation?	2	2	1,2	1,2
12. a)	Find Zbus for the system shown in fig. 	4	5	2	1,2
b)	Explain the algorithm for formation of Zbus matrix	4	2	3	1,2

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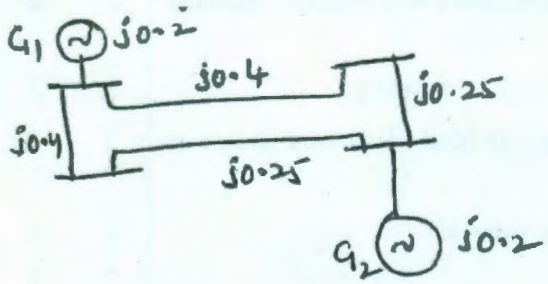
Code No. : 21712

13. a)	With the help of flowchart, explain how to obtain load flow solution using Fast decoupled load flow method?	5	2	3	1,3, 4
b)	Explain the classification of buses in load flow studies.	3	2	3	1,2
14. a)	Explain an algorithm for formation of three-phase bus impedance matrix for addition of branch?	5	4	3	1,3, 4
b)	What are transformation matrices and write their significance.	3	2	2	1,2
15. a)	Derive the expressions for fault currents, voltages when 3-phase to ground fault occurs at bus P. Also write flowchart?	5	4	1,2	1,2
b)	What are the basic assumptions made in short circuit studies.	3	2	2	1,2
16. a)	For the network shown in fig., obtain the bus admittance matrix by singular transformation? 	5	5	1,2	1,2
b)	What are the advantages of Zbus building algorithm?	3	2	1,2	1,3
17.	Answer any ***two*** of the following:				
a)	Compare the various methods of load flow study?	4	1	1,2	1,3
b)	Show that impedance matrix is same both in symmetrical components and Clark's components for a balanced three-phase stationary elements?	4	2	1,2	1,2
c)	Derive Z_F^{abc} for LLG fault on phases b and c?	4	3	1,2	1,2

M: Marks; L: Bloom's Taxonomy Level; CO: Course Outcome; PO: Programme Outcome

S. No.	Criteria for questions	Percentage
1	Fundamental knowledge (Level-1 & 2)	58.75
2	Knowledge on application and analysis (Level-3 & 4)	30.0
3	*Critical thinking and ability to design (Level-5 & 6) (*wherever applicable)	11.25

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Hall Ticket Number:

Code No. : 21714

VASAVI COLLEGE OF ENGINEERING *(Autonomous)*, HYDERABAD

M.E. (EEE: CBCS) I-Semester Main Examinations, January-2019

(Power Systems & Power Electronics)

Application of Power Electronics to Power Systems

Time: **3** hours Max. Marks: **60**

*Note: Answer **ALL** questions in **Part-A** and any **FIVE** from **Part-B***

Q. No	Stem of the Question	M	L	CO	PO
	Part-A (10 × 2 = 20 Marks)				
1.	What is meant by Flexible AC Transmission Systems?	2	1	1	1
2.	Explain how transmission interconnection will improve stability.	2	2	1	1-2
3.	Define the term Static VAR Compensator.	2	2	2	1
4.	Identify the factors to be considered for designing SVC to regulate midpoint voltage.	2	4	2	1-2
5.	Draw the V-I characteristics of TCSC.	2	1	3	1-3
6.	List the types of variable series compensation techniques.	2	1	3	1-2
7.	Give the basic block diagram of UPFC.	2	2	4	1
8.	Demonstrate how reactive power compensation can be done through combined controllers.	2	3	4	1-3
9.	What is the role of active filters in harmonic mitigation?	2	1	5	1
10.	List the power quality issues as per IEEE standards.	2	1	5	1
	Part-B (5 × 8 = 40 Marks)				
11. a)	Explain loading capability limits and dynamic stability considerations of FACTS controllers.	4	2	1	1-2
b)	List the benefits of FACTS controllers.	4	4	1	1-2
12. a)	Discuss the operation of SVC with neat circuit diagram. Draw its V-I characteristics.	5	2,6	2	1-3
b)	Write short notes on operation of STATCOM.	3	1	2	1-2
13. a)	With basic scheme and characteristics, explain the operation of TCSC.	4	2	3	1-2
b)	Discuss the operation of SSSC with help of one line diagram.	4	2,6	3	1-3
14. a)	Explain the operation of UPFC for stability studies.	5	2	4	1-3
b)	Write the salient features of UPFC.	3	2	4	1-3
15. a)	List the advantages of hybrid filters over active filters.	4	2	5	1-2
b)	Describe how filters can be used in power system networks for mitigation of harmonics.	4	4	5	1-4,12
16. a)	What is voltage instability? How it can be tackled by end of line compensation.	4	3	2	1-4
b)	Discuss about different FACTS controllers.	4	1	1	1-4,12
17.	Answer any *two* of the following:				
a)	Analyze the performance characteristics of GCSC.	4	4	3	1-4
b)	Compare UPFC and series compensators.	4	2	4	1-3
c)	Describe the role of passive filters in oscillation damping.	4	6	5	1-4

M: Marks; L: Bloom's Taxonomy Level; CO: Course Outcome; PO: Programme Outcome

S. No.	Criteria for questions	Percentage
1	Fundamental knowledge (Level-1 & 2)	70%
2	Knowledge on application and analysis (Level-3 & 4)	22.5%
3	*Critical thinking and ability to design (Level-5 & 6) (*wherever applicable)	7.5%